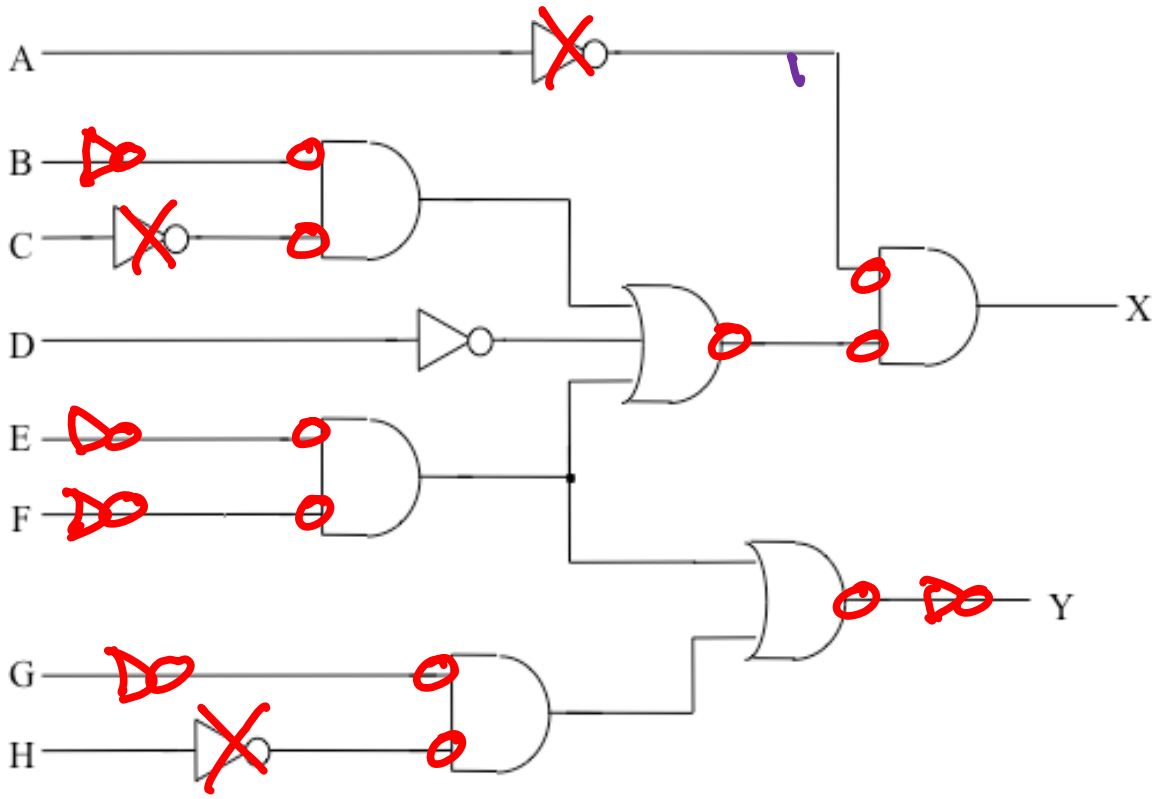
CSE 369 Autumn 2015 – Quiz 1 (3 November)

Name:

Problem	Max Score	Score
1	10	
2	10	
3	10	
TOTAL	**30**	

1. Logic gates (10 points)

Modify the following circuit diagram such that the final circuit uses only NOR and NOT gates. Use the minimal necessary number of additional gates.



2. Verilog (10 points)

Briefly explain what this module does. Describe the overall function in one sentence and add 1-2 brief comments into the code to explain salient features.

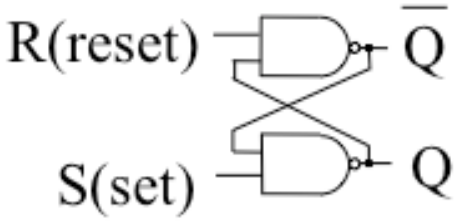
```
module Unknown (C, D, E, A, B);
  input     A, B;
  output    C, D, E;

  assign #5 C   = (A & B) | (~A & ~B);
  assign #3 D = (A & ~B);
  assign #3 E = (~A & B);
endmodule
```

TRUE IF A=B
A>B
A<B

"COMPARATOR" CIRCUIT

3. Storage element (10 points)
Create the truth table for the storage element shown below. What is the value of Q for every combination of the inputs R and S? Briefly explain your reasoning.



IF ONE INPUT TO A NAND GATE IS "0" THE OUTPUT IS ALWAYS "1"

IF BOTH INPUTS ARE "1" ASSUME Q=0 (OR Q=1), THEN CHECK FOR CONSISTANCY.

R	S	Q	$\overline{Q}$
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Q	~Q

(SR-LATCH)